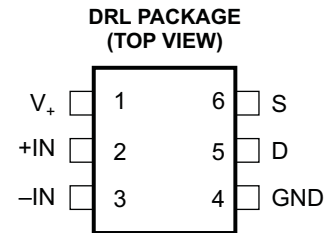


FEATURES

- **Low Supply Current: 8 μ A (Max)**
- **Supply Voltage: 3 V to 5.5 V**
- **Output FET Provides Down Translation**
- **Small Package: SOT-563**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance**
 - **2500-V Human-Body Model (IEC61340-3-1:2002 Level 2)**
 - **250-V Machine Model (IEC61340-3-2 Level M2)**
 - **1500-V Charged-Device Model (JESD22-C101-A Level III)**



DESCRIPTION/ORDERING INFORMATION

The TXS03121 is a comparator designed for battery monitoring applications. It can be operated with a voltage of 3 V to 5.5 V. The reference voltage is applied to the –IN terminal, whereas the voltage to be monitored is connected to +IN. When the voltage at +IN is greater than the voltage at –IN, the output FET is turned On. When the voltage at +IN is less than the voltage at –IN, the output FET is turned Off. The source (S) of the output FET can be connected to 1.1 V to 3.6 V, which allows the output signal to be level translated to another voltage value. The voltage at V₊ must be greater than or equal to the voltage at S. The voltage at S must be greater than or equal to the voltage at D ($V_+ \geq V_S \geq V_D$).

ORDERING INFORMATION

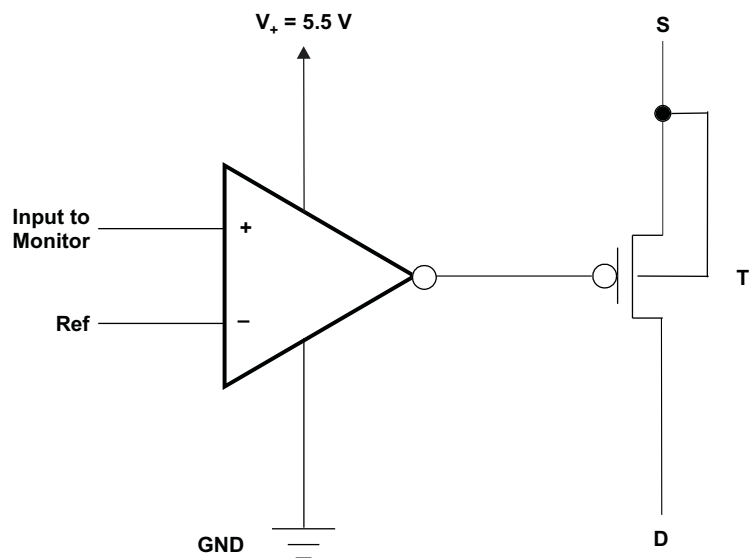
T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	DRL (SOT-563)	Tape and reel	TXS03121DRLR	2FR

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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APPLICATION BLOCK DIAGRAM



PIN ASSIGNMENTS

NO.	NAME	DESCRIPTION
1	V_+	Comparator supply voltage
2	+IN	Comparator positive input
3	-IN	Comparator negative input
4	GND	Ground
5	D	Drain of output FET
6	S	Source of output FET

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V ₊	Supply voltage range ⁽²⁾		-0.5	6.5	V
+IN, -IN	Input voltage range		-0.5	6.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current (On-state switch current)			±50	mA
	Continuous current through V ₊ or GND			±100	mA
θ _{JA}	Package thermal impedance ⁽³⁾	DRL package		171.6	°C/W
T _{stg}	Storage temperature range			150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V ₊	Comparator supply voltage	3	5.5	V
V _S , V _D ⁽¹⁾	Output FET source or drain voltage	1.1	3.6	V
T _A	Operating free-air temperature	-40	85	°C

- (1) V₊ must be greater than or equal to V_S, and V_S must be greater than or equal to V_D (V₊ ≥ V_S ≥ V_D).

TXS03121 COMPARATOR WITH OUTPUT VOLTAGE-LEVEL TRANSLATION

SCES680–JULY 2007

Comparator Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

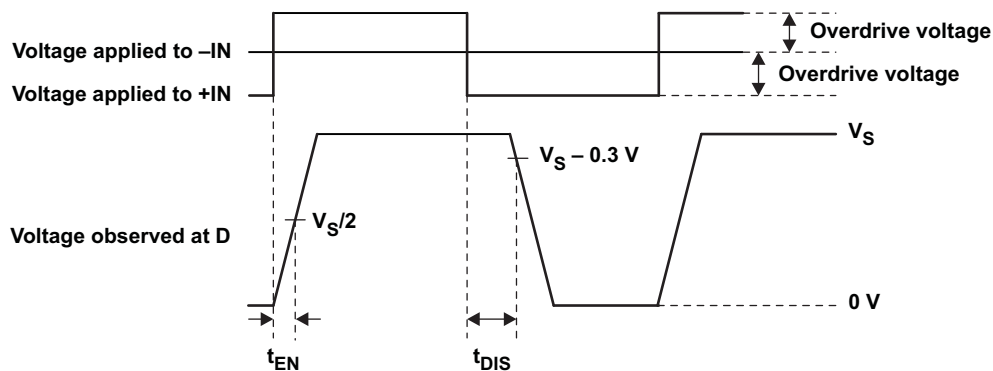
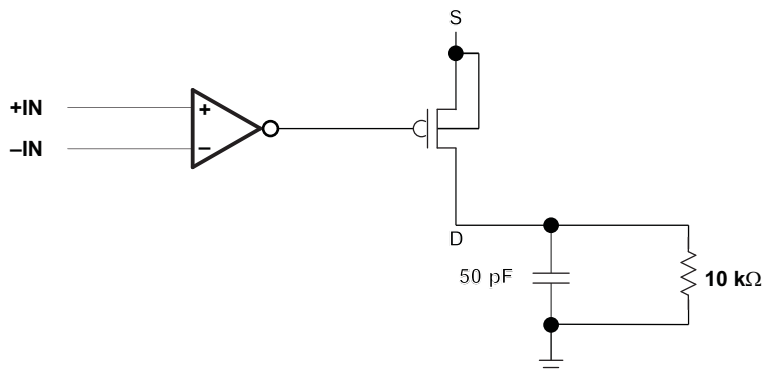
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OS}	Input offset voltage	V ₊ = 3 V to 5.5 V	V _{CM} = 0.8 V, I _O = 0	–10	0.5	10	mV
			V _{CM} = V ₊ , I _O = 0				
V _{CM}	Common-mode voltage range	V ₊ = 3 V to 5.5 V		0.8		V ₊	V
I _{+IN}	Input leakage current	V ₊ = 3 V to 5.5 V	V _{+IN} = 0 V to V ₊			0.5	μA
I _{-IN}			V _{-IN} = 0 V to V ₊				
I ₊	Supply current	V ₊ = 3 V to 5.5 V				8	μA
C _{IN}	Capacitance of +IN, –IN pins				2	2.5	pF

Output FET Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$I_{DS(ON)}$	On leakage current	$V_S = 1.1\text{ V to }3.6\text{ V}$, Switch ON				0.5	μA	
$I_{DS(OFF)}$	Off leakage current	$V_S = 1.1\text{ V to }3.6\text{ V}$, $V_D = \text{Open}$, Switch OFF				0.5	μA	
$C_{(ON)}$	On capacitance			4	5.1	6	pF	
$C_{(OFF)}$	Off capacitance, S and D terminals			1.5	3.4	5	pF	
R_{ON}	On resistance of output FET	$V_+ \geq V_S$, $I_D = 100\ \mu\text{A}$		$V_S = 1.1\text{ V}$		150	Ω	
				$V_S = 1.4\text{ V}$		65		
				$V_S = 1.65\text{ V}$		61		
				$V_S = 2.3\text{ V}$		50		
				$V_S = 3\text{ V}$		44		
t_{EN}	Enable time	20-mV overdrive	$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$,		6.6	μs	
				$V_+ = 3\text{ V}$		15		
			$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		2.5		
				$V_+ = 3\text{ V}$		12.6		
			50-mV overdrive	$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$			1.6
					$V_+ = 3\text{ V}$			4.1
		$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$		$V_+ = 4.5\text{ V}$		1		
				$V_+ = 3\text{ V}$		3.1		
		100-mV overdrive		$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$			0.8
					$V_+ = 3\text{ V}$			2.4
			$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		0.7		
				$V_+ = 3\text{ V}$		2.2		
t_{DIS}	Disable time	20-mV overdrive	$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		10.9	μs	
				$V_+ = 3\text{ V}$		17.4		
			$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		4.2		
				$V_+ = 3\text{ V}$		6.8		
			50-mV overdrive	$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$			13
					$V_+ = 3\text{ V}$			15.4
		$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$		$V_+ = 4.5\text{ V}$		2.8		
				$V_+ = 3\text{ V}$		5.2		
		100-mV overdrive		$V_{-IN} = 0.8\text{ V}$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$			16.1
					$V_+ = 3\text{ V}$			16.4
			$V_{-IN} = V_+$, $V_S = 1.65\text{ V}$	$V_+ = 4.5\text{ V}$		1.9		
				$V_+ = 3\text{ V}$		4		

PARAMETER MEASUREMENT INFORMATION



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TXS03121DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TXS03121DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS03121DRLR	SOT	DRL	6	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

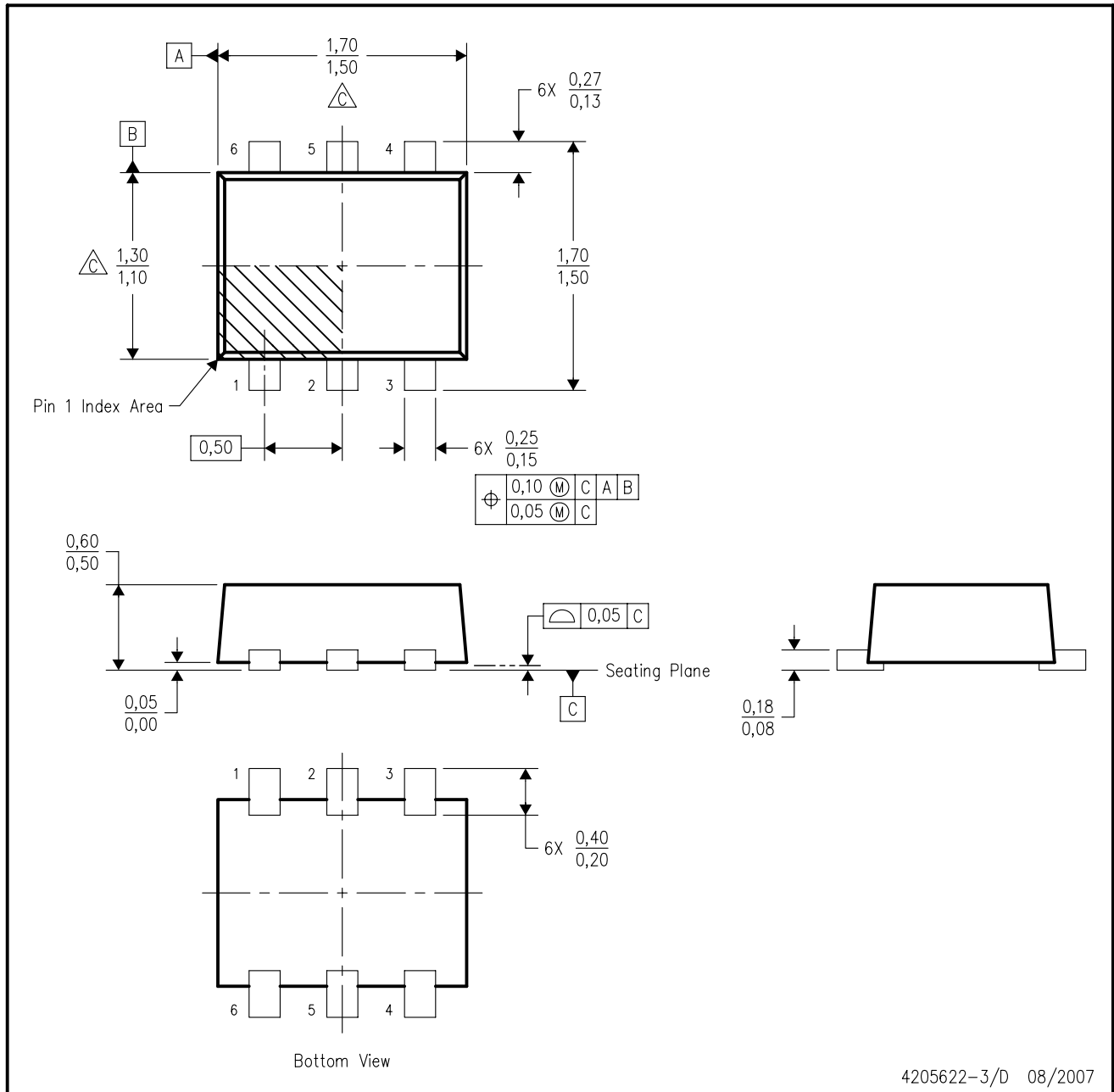


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS03121DRLR	SOT	DRL	6	4000	202.0	201.0	28.0

DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



4205622-3/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

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